AMENDMENTS TO THE CLAIMS

Listing of claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1-22. (Canceled)

23. (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulating film formed on said semiconductor substrate;

a gate electrode of a MIS transistor formed on said gate insulating film;

first and second impurity diffusion regions constituting source and ~~rain~~ drain of said MIS transistor formed in said semiconductor substrate on both sides of said gate electrode;

a first insulating film formed on said semiconductor substrate inclusive of said gate electrode and said first and second impurity diffusion regions;

a second insulating film of a silicon nitride film formed on said first insulating film;

first and second contact ~~areas~~ holes formed in and through said first and second insulating films and respectively reaching said first and second impurity diffusion regions;

first and second conductive ~~layers formed~~ plugs embedded in said first and second contact ~~areas~~ holes and connected to said first and second impurity diffusion regions,

respectively, an upper surface of the first and second conductive plugs being substantially at the same level with an upper surface of the second insulating film;

a third insulating film formed on said second insulating film and the upper surface of the first and second conductive plugs;

a third contact ~~area~~ hole formed through said third insulating film and reaching said first conductive ~~layer~~ plug; and

a ~~third~~ first conductive layer connected to said first conductive ~~layer~~ plug via said third contact ~~area~~ hole.

24. (Currently Amended): A semiconductor device according to claim 23, further comprising:

a ~~fourth~~ first contact area formed through said third insulating film and reaching said second conductive ~~layer~~ plug;

a ~~fourth~~ second conductive layer constituting a storage electrode connected to said second conductive ~~layer~~ plug via said ~~fourth~~ first contact area; and

a ~~fifth~~ third conductive layer constituting an opposing electrode formed to face said ~~fourth~~ second conductive layer, with a capacitor insulating film being interposed between said ~~fourth~~ second and ~~fifth~~ third conductive layers.

25. (Currently Amended): A semiconductor device according to claim 24, wherein said ~~fourth~~ second conductive layer has a bottom portion and a cylindrical portion vertical to said semiconductor substrate.

26. (Currently Amended): A semiconductor device according to claim 23, wherein said third contact ~~area~~ hole extends to an area over said second insulating film formed at the outside of said first conductive ~~layer~~ plug.

27. (Currently Amended): A semiconductor device according to claim 24, wherein said ~~fourth~~ first contact area extends to an area over said second insulating film formed at the outside of said second conductive ~~layer~~ plug.

28. (Currently Amended): A semiconductor device according to claim 24, wherein part of the bottom portion of said ~~fourth~~ second conductive layer is in contact with an upper portion of said second insulating film.

29. (Currently Amended): A semiconductor device according to claim 24, wherein said end portion of said ~~fifth~~ third conductive layer and the end portion of said second insulating film are registered in a plan view.

30. (Currently Amended): A semiconductor device according to claim 23, further comprising a fourth insulating film made of a silicon nitride film and formed on said ~~third~~ first conductive layer, wherein said fourth insulating film is thicker than said second insulating film.

31. (Original): A semiconductor device comprising:

a semiconductor substrate;

a gate insulating film formed on said semiconductor substrate;

a gate electrode of a MIS transistor formed on said gate insulating film;

impurity diffusion regions constituting a source and a drain of said MIS transistor formed in said semiconductor substrate on both sides of the gate electrode;

a first insulating film formed on said semiconductor substrate inclusive of said gate electrode and said impurity diffusion regions;

a first contact area formed through said first insulating film and reaching at least one of said impurity diffusion regions;

a first conductive layer formed in said first contact area and connected to one of said impurity diffusion regions;

a second insulating film formed on said first insulating film;

a third insulating film of a silicon nitride film formed on said second insulating film;

a second contact area formed in and through said second and third insulating films and reaching said first conductive layer;

a second conductive layer constituting a storage electrode connected to said first conductive layer via said second contact area, said second conductive layer having a bottom portion and a cylindrical portion vertical to said semiconductor substrate; and

a third conductive layer facing said second conductive layer with a capacitor insulating film being interposed therebetween, part of said third conductive layer being in contact with the surface of said third insulating film via the capacitor insulating film.

32. (Original): A semiconductor device according to claim 31, wherein the end portion of said third conductive layer and the end portion of said third insulating film are registered in a plan view.

33-37. (Canceled)

38. (Previously Presented): A semiconductor comprising:

a semiconductor substrate having a surface;

first and second conductive layers formed at levels different in distance from the substrate surface, the levels becoming higher in the order of the first and second conductive layers;

a first insulating film formed on said substrate, covering said first and second conductive layers;

a first contact area formed through said first insulating film and exposing the top surface of said first conductive layer;

a second contact area formed in and through said first insulating film and said second conductive layer, said second conductive layer having a side wall exposed in said second contact area; and

a pair of third conductive layers formed at least in said first and second contact areas and connected via said first contact area to the surface of said first conduction layer and to the side wall of said second conductive layer via said second contact area,

wherein D1 is larger than D2, where D1 is a depth from the surface of said first insulating film to said first conductive layer and D2 is a depth from the surface of said first insulating film to said second conductive layer,

wherein said second conductive layer is a capacitor opposing electrode of a capacitor.

39-41. (Canceled)

42. (Previously Presented): A semiconductor device comprising:

a semiconductor substrate having a surface;

first to third conductive layers formed at levels different in distance from the substrate surface, the levels becoming higher in the order of the first, third, and second conductive layers;

a first insulating film formed on said substrate inclusive of said first to third conductive layers;

a second insulating film formed under said second conductive layer and having etching characteristic different from said first insulating film;

a third insulating film formed to cover said third conductive layer and having etching characteristics same as said second insulating film;

a first contact area formed through said first insulating film and exposing the top surface of said first conductive layer;

a second contact area formed through said first insulating film, said second conductive layer, and said second insulating film, said second conductive layer having a side wall exposed in said second contact area;

a third contact area formed through said first and third insulating films and exposing the surface of said third conductive layer; and

three fourth conductive layers respectively connected to the surface of said first conductive layer via said first contact area, to the side wall of said second conductive layer via

said second contact area, and to the surface of said third conductive layer via said third contact area,

wherein D1 > D3 > D2, there D1 is a depth from the surface of said first insulating film to said first conductive layer, D2 is a depth from the surface of said first insulating film to said second conducive layer, and D3 is a depth from the surface of said first insulating film to said third conductive layer,

wherein said second conductive layer is a capacitor opposing electrode of a capacitor.

43. (Original): A semiconductor device comprising:

a semiconductor substrate having a surface;

a plurality of first conductive layers formed on the surface of said semiconductor substrate generally parallel;

first insulating films formed to cover said first conductive layers;

a second insulating film embedded between adjacent ones of said first conductive layers, said second insulating film having a surface coincident with the upper surface of said first insulating films and parallel to the surface of said semiconductor substrate; and

a contact area formed in said second insulating film, part of said contact area riding upon one of said first insulating films.

44. (Original): A semiconductor device according to claim 43, wherein said first conductive layers form a DRAM bit lines.

45. (Previously Presented): A semiconductor device comprising:

a semiconductor substrate having a surface;

a plurality of first conductive layers formed on the surface of said semiconductor substrate generally in parallel and having a plurality of levels different in distance from the surface of said semiconductor substrate;

first insulating films formed to cover said first conductive layers; and

a second insulating film embedded between adjacent ones of said first conductive layers and having a surface coincident with the upper surface of said first insulating films with the highest level in distance from the surface of said semiconductor substrate and parallel to the surface of said semiconductor substrate.

46. (Original): A semiconductor device according to claim 45, further comprising a contact area formed in said second insulating film, part of said contact area extending to an area over one of said first insulating films.

47. (Original): A semiconductor device according to claim 45, wherein said first insulating films are each made of a silicon nitride film.

48. (Original): A semiconductor device according to claim 45, wherein said semiconductor substrate includes a field insulating film defining active regions, said first conductive layers with the highest level in distance from the surface of said semiconductor substrate are formed on the field insulating film, and said first conductive layers with the lowest level in distance from the surface of said semiconductor substrate are formed on the active regions.

49. (Original): A semiconductor device according to claim 48, wherein said first conductive layer is a DRAM word line.

50. (Original): A semiconductor device comprising:

a silicon substrate having a surface;

a gate insulating film formed on said silicon substrate;

a gate electrode of a MIS transistor formed on said gate insulating film;

first and second impurity diffusion regions constituting source and drain of said MIS transistor formed in said silicon substrate on both sides of said gate electrode;

an insulating film formed on said silicon substrate inclusive of said gate electrode and said first and second impurity diffusion regions;

a pair of contact areas formed in and through said insulating film and reaching said first and second impurity diffusion regions;

first and second conductive layers made from the same conductive layer and connected to said first and second impurity diffusion regions via said contact area;

a bit line connected to said first impurity diffusion area via said first conductive layer; and

a capacitor storage electrode connected to said second impurity diffusion region via said second conductive layer,

wherein the impurity concentration of said second impurity diffusion region is larger than the impurity concentration of said first impurity diffusion region.

51. (Original): A semiconductor device comprising:

a silicon substrate having a surface;

a gate insulating film formed on said silicon substrate;

a gate electrode of a MIS transistor formed on said gate insulating film;

first and second impurity diffusion regions constituting source and rain of said MIS transistor, having the same impurity concentration and formed in said silicon substrate on both sides of said gate electrode;

an insulating film formed on said silicon substrate inclusive of said gate electrode and said first and second impurity diffusion regions;

a pair of contact areas formed through said insulating film and reaching said first and second impurity diffusion regions;

a third impurity diffusion region of the same conductivity type as said second impurity diffusion region formed in said silicon substrate under said contact area merging with said second impurity diffusion region, the impurity concentration of said third impurity diffusion region is larger than the impurity concentration of said first and second impurity diffusion regions;

a first conductive layer connected to said first impurity diffusion area via one of said contact areas;

a second conductivity layer made from the same conductive layer as said first conductive layer and connected to said second impurity diffusion region and said third impurity diffusion region via the other of said contact areas;

a bit line connected to said first impurity diffusion region via said first conductive layer; and

a capacitor storage electrode connected to said second impurity diffusion region via said second conductive layer.

52-61. (Canceled)